

Simplified Design of An FPGA-Accelerated Connectionless Network Stack

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Nowadays, one of the most discussed technology-related issues in the networking domain is how a highly performant and easily accessible to everyone implementation can look like. To reach this target, hardware acceleration comes into the game by offering high performance, programmability capabilities, and a minimal design of a network protocol stack. The Field-Programmable Gate Array (FPGA) is the most chosen hardware solution for such an implementation. Currently, there are multiple research directions in which the programming language to Hardware Description Languages (HDL) tools are used. However, there is a lack of research in the softwarization for the hardware-accelerated network protocol stack. Therefore, this paper proposes a simplified network protocols design by leveraging on Tom's Obvious Minimal Language (TOML) configuration language. We evaluated the approach by using a TCP/IP along with the integration into a 10 Gigabit Ethernet-like device and the use of Advanced eXtensible Interface (AXI) Streaming-based data generator.

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