Design and Validation of an Extended FPGA-Based HC-85 Architecture

For Computer Architecture Education

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Motivation and contribution

A complete computer students can trace

Historical software

Original HC-85 BASIC runs on a reused Z80-compatible T80 core.

Serial extension

UART characters enter through the existing keyboard matrix, without a ROM patch.

Teaching focus: processor buses, memory organization, interrupts, and peripheral protocols

System architecture

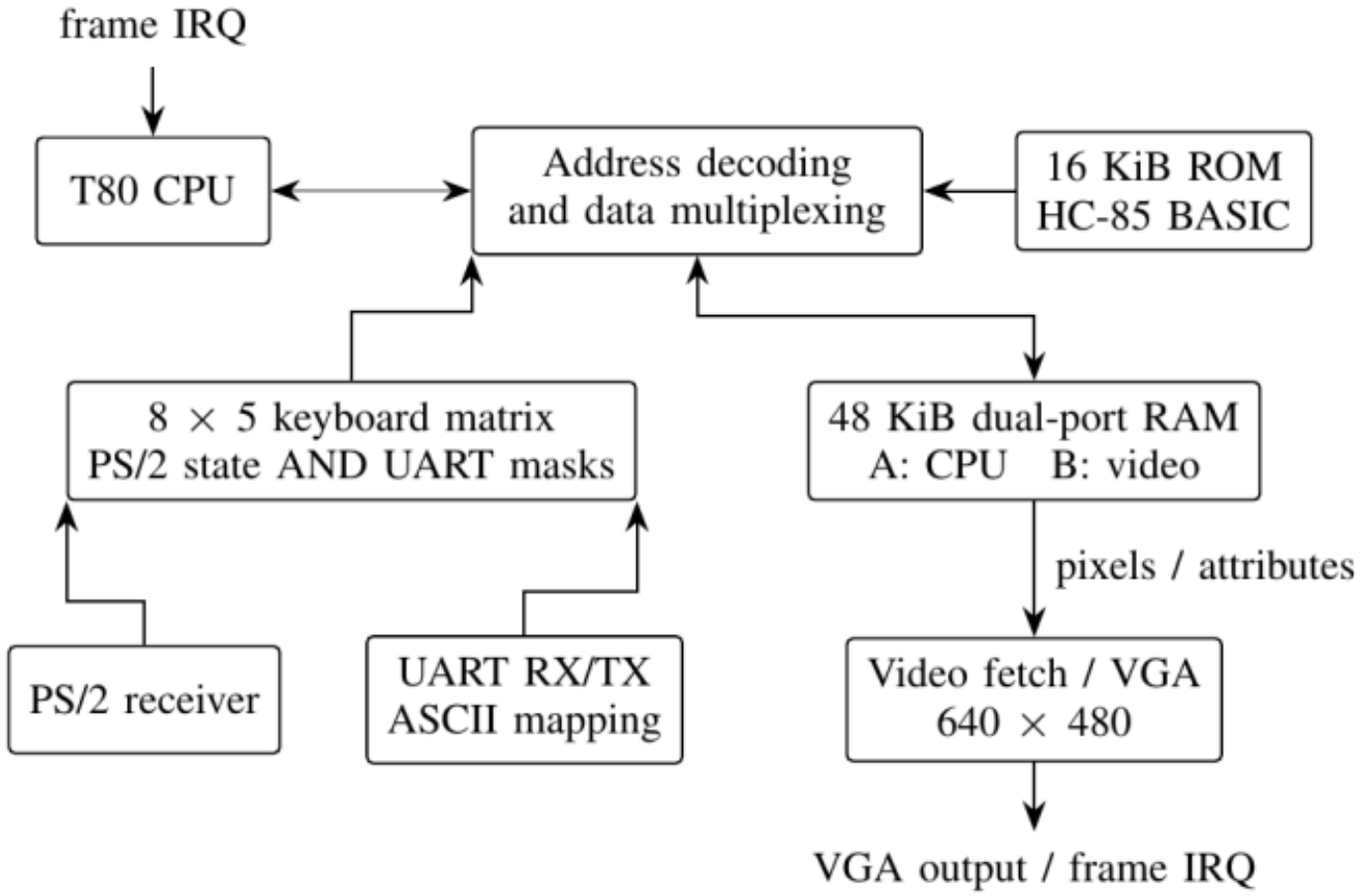
Digilent Nexys3

Spartan-6 XC6SLX16

100 MHz system clock

16-bit address bus
8-bit data paths

All memory on chip



Memory map and concurrent access

Address range	Capacity	Purpose
0x0000–0x3FFF	16 KiB	BASIC ROM
0x4000–0x57FF	6,144 B	Display bitmap
0x5800–0x5AFF	768 B	Display attributes
0x5B00–0xFFFF	42,240 B	Remaining RAM

48 KiB true dual-port RAM

Independent CPU and video ports remove display contention.
Program addresses remain unchanged, while access timing changes.

Processor and display timing

3.571 MHz

CPU advancement: 100 MHz / 28
About 2.04% above the 3.5 MHz target

59.52 Hz

VGA frame and interrupt rate
25 MHz / (800 × 525)

Frame interrupts drive periodic ROM tasks, including keyboard scanning

Functional interpreter compatibility is the validation target.
Whole-system cycle equivalence is outside the demonstrated scope.

VGA display adaptation

256 × 192

Original bitmap, with a 32 × 24 attribute grid

Scaled VGA image

2× scaling on each axis gives 512 × 384 pixels inside a 640 × 480 region.

Color and border

Eight colors and FLASH. Writes to port 0xFE select the border color.

Original bitmap addressing lets the ROM draw directly into display memory

Physical and serial keyboard input

PS/2 keyboard

Scan codes reconstruct the 40-key, active-low HC-85 matrix.

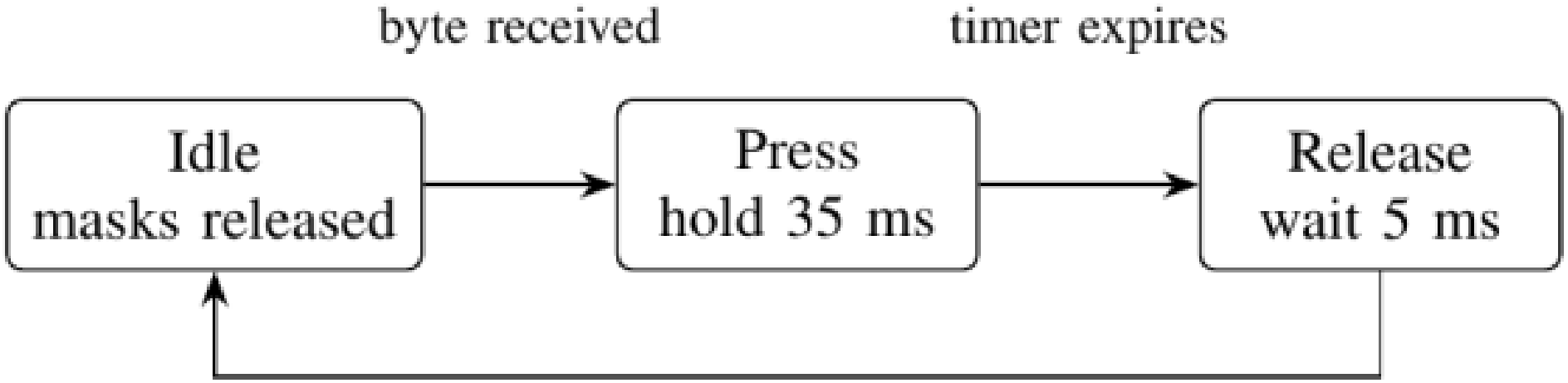
UART terminal

Supported ASCII characters generate key and modifier masks.

Returned row = PS/2 state AND UART mask

The ROM reads the same eight-by-five matrix through port 0xFE.
Both input sources use the interpreter’s existing scanning routine.

UART key-event timing



115200 baud, 8N1

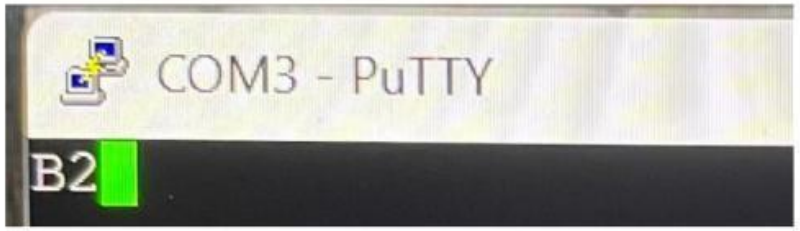
35 ms press + 5 ms release

Nominal ceiling: 25 key events/s. Sustained loss-free throughput and buffering during busy states remain unverified.

Hardware validation



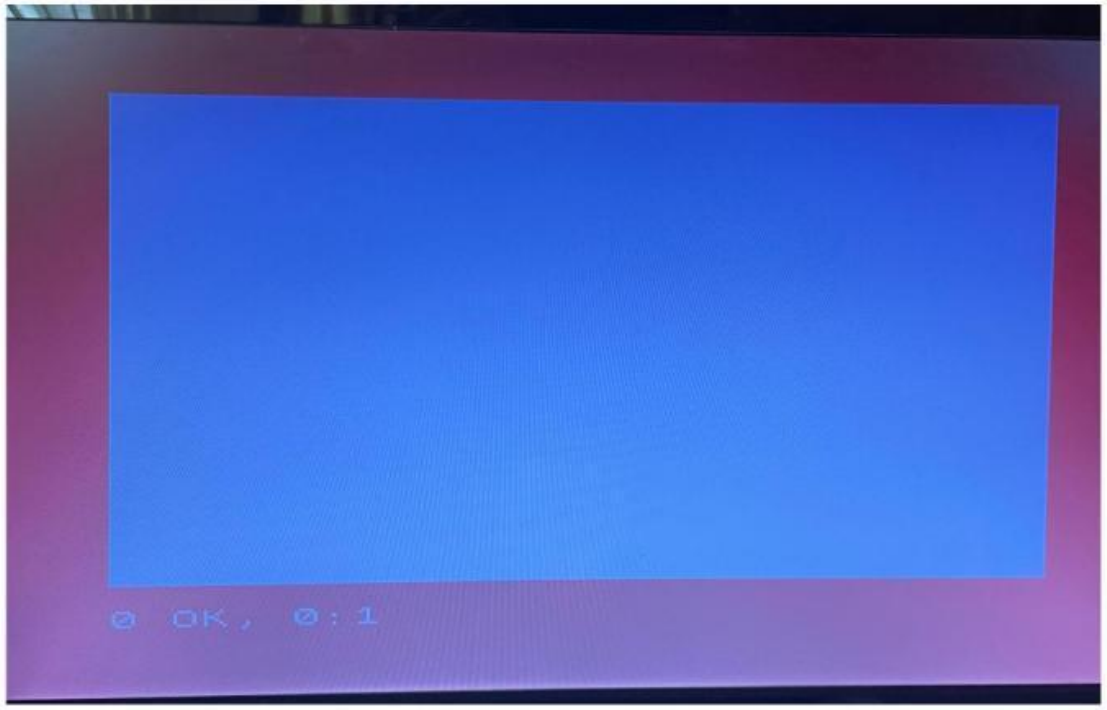
(a) BASIC startup identification (detail).



(b) PuTTY input: `B2`.



(c) BASIC input line: `BORDER 2` (PS/2 demonstration).



(d) Display after command execution: changed border.

Test ROM checks precede full-system testing with original BASIC.
Startup, all 40 keys, interactive UART input, and color display were observed.

Block RAM is the limiting resource

Resource	Used	Available	Utilization
Slice registers	668	18,224	3.67%
Slice LUTs	2,077	9,112	22.79%
Occupied slices	733	2,278	32.18%
RAMB16BWER blocks	32	32	100.00%

64 KiB of ROM + RAM consumes all reported block memory

Memory-intensive extensions need external memory, a revised allocation,
or a larger device.

Proposed laboratory activities

Topic	Student-produced evidence
Address decoding	Boundary waveforms at 0x3FFF and 0x4000
Memory and display	CPU/video access traces and pixel-address checks
Interrupts and serial input	8N1 decoding, matrix masks, paced/repeated-key tests
Resource tradeoffs	Buffering or peripheral design with synthesis reports

A BORDER command connects input reception to visible computer behavior

Educational effectiveness remains a question for a future classroom study

Conclusions and next steps

A functional HC-85 reconstruction with an unmodified BASIC ROM

UART extends input through the existing keyboard matrix.
Dual-port RAM separates processor and display access.

Next steps

Versioned release and complete build evidence
Measured timing and UART robustness
Buffered program transfer and broader software testing